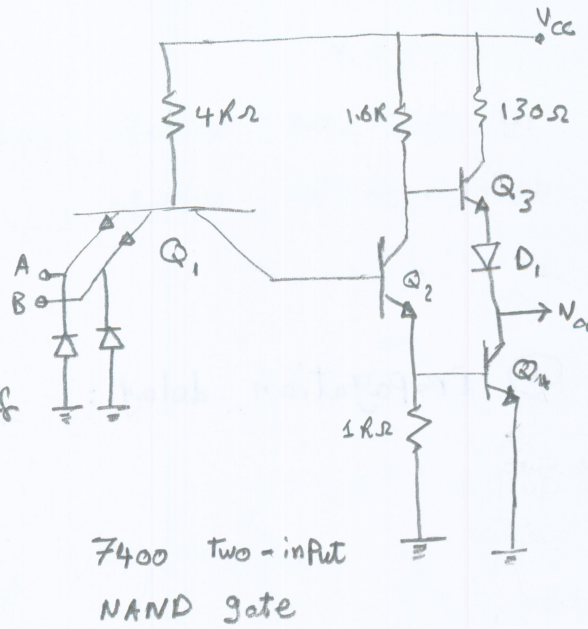
Digital Lec (2) 4/10/2016

⊛ TTL family :

- TTL Voltage / Current Rating



7400 two-input NAND gate

A = 0
B = 0 or each is 0 ⟹ Vout = high stat

Q_3 → ON Q_4 ⇒ off

Source current (I_{OH})

= − 400 μA

A = 1
B = 1 ⟹ Vout = Low stat (logic 0)

Q_3 → off Q_4 → ON

Sink current (I_{OL})

= 16 mA

I_{ih} = 40 μA

I_{iL} = − 1.6 mA

* Fan-out (Low-stat) $= \frac{|I_{OL}|}{|I_{IL}|} = \frac{16\,mA}{1.6\,mA} = 10$ gates

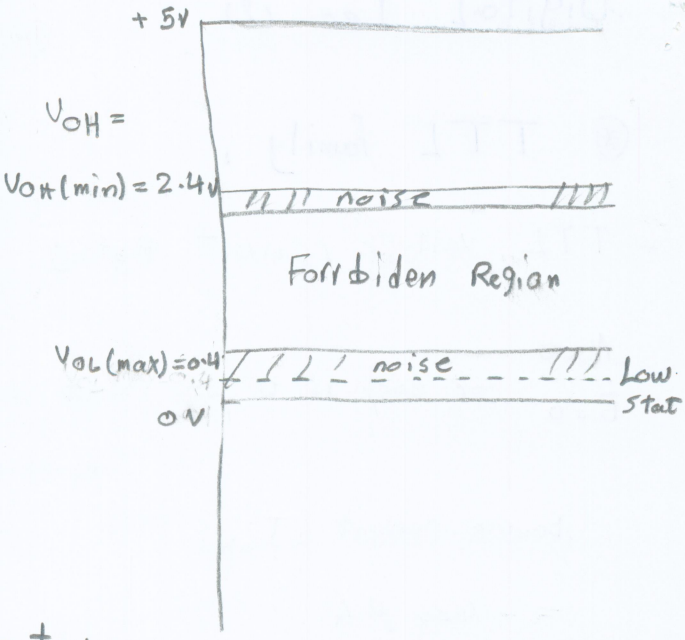
* Fan-out (high-stat) $= \frac{|I_{OH}|}{|I_{IH}|} = \frac{400\,\mu}{40\,\mu} = 10$ gates

(*) Noise Margin

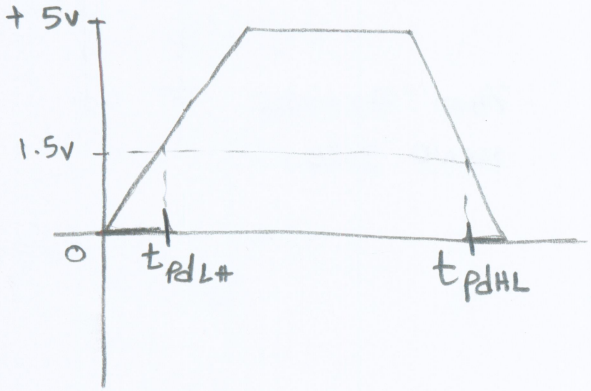
= 0.4 V

up Low - stat voltage (0v: 0.8v)

down high stat voltage (2v: 5v)



(*) Propagation delay :



$t_{pdLH} = t_{pdHL}$ = 10 n sec

(*) Rise time t_r

Time of 10% : 90% of full voltage

0.5 V : 4.5 V

(*) Fall time t_f

time of 90% : 10% of full voltage

4.5 V : 0.5 V

Power Dissipation :

$P_D = V_{cc} * I_{cc}(av)$

$I_{cc}(av) = \frac{I_{cc\#} + I_{ccL}}{2}$